

REMARKS

Claims 1-4 and 6-12 remain pending in this application. Claim 5 has been canceled, without prejudice or disclaimer of subject matter. Claims 1-4 and 6-11 have been amended to define still more clearly what Applicant regards as his invention. Favorable reconsideration is requested.

Applicant has corrected the informalities kindly pointed out by the Examiner at paragraph 1 of the Office Action.

Claims 1-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,266,450 to Yip et al.

First, cancellation of Claim 5 renders the rejection of that claim moot

Claim 1 is directed to a data transfer circuit for transferring a data group having data represented by plural bits from a first memory to a second memory for coding by a bit-plane coding processor. Detection means detects a maximum value in the data group as a transfer object, wherein the detecting processing by the detection means is performed while transferring the data group and completed before completion of the transfer. Specifying means specifies a non-zero highest-order bit position among bits constructing the maximum value detected by the detection means, and outputs a code representing the bit position specified by the specifying means to the bit-plane coding processor. A bit in a position higher than the highest-order bit position specified by the specifying means is omitted from coding by the bit-plane coding processor.

Therefore, Claim 1 is directed to a data transfer circuit (e.g., DMA circuit

12 of Applicant's Fig. 1) which transfers data between two memories in an encoding system.^{1/} The data transfer circuit specifies a position of a bit plane to be encoded (or not encoded) while transferring data from a first memory (e.g., main memory 16) to a second memory (e.g., coding buffer memory 10). Thus, since a bit-plane coding processor (e.g., a bit plane coding processor 11) can acquire a position of a bit plane to be encoded (or not encoded) before the bit-plane coding processor reads out data of the second memory and encodes the read data, the encoding processing can be performed quickly.

Yip et al. relates to an apparatus for the encoding of a series of wavelet coefficients of a predetermined size into a compact representation of the coefficients. The apparatus comprises a tree builder for constructing a tree form representation of the coefficients with leaf nodes representing coefficient values and internal nodes representing the number of bits needed to encode leaf nodes and child nodes of a current internal node. The tree builder stores the tree form representation in a tree buffer of the apparatus, and the tree buffer stores the tree form representation. A tree coder of the apparatus is interconnected to the tree buffer and adapted to read a current tree form representation and to output the encoding from the tree form representation. The tree buffer can include a component for storing at least two tree form representations and the tree builder can be adapted to form a first of the representations while the tree coder can be adapted to read a second of the tree form representations previously created by the tree builder.

Yip et al. does not teach or suggest that a data transfer circuit, which

^{1/}It is of course to be understood that the references to various portions of the present application are by way of illustration and example only, and that the claims are not limited by the details shown in the portions referred to.

transfers data between a first memory to a second memory, specifies a position of a bit plane to be encoded (or not encoded) upon transferring. That is, nothing in Yip et al. would teach or suggest a data transfer circuit for transferring a data group from a first memory to a second memory for coding by a bit-plane coding processor, including “detection means for detecting a maximum value in the data group as a transfer object, wherein the detecting processing by said detection means is performed while transferring the data group and completed before completion of the transfer”, and “specifying means for specifying a non-zero highest-order bit position among bits constructing the maximum value detected by said detection means, and outputting a code representing the bit position specified by said specifying means to said bit-plane coding processor”, “wherein a bit in a position higher than the highest-order bit position specified by said specifying means is omitted from coding by said bit-plane coding processor,” as recited in Claim 1.

Accordingly, Claim 1 is seen to be clearly allowable over Yip et al.

Independent Claims 2-4 and 8-11 recite features similar in many respects to those discussed above with respect to Claim 1, and therefore are also believed to be patentable over Yip et al. for at least the same reasons discussed above.

A review of the other art of record has failed to reveal anything which, in Applicant’s opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

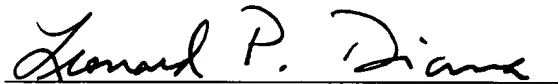
The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the

same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

A handwritten signature in cursive script, reading "Leonard P. Diana", is written over a horizontal line.

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